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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,172	01/22/2000	Deborah T. Marr	2207/7942	6827

7590 01/06/2006

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EXAMINER	
CHEN, TE Y	

ART UNIT	PAPER NUMBER
2161	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/490,172	MARR, DEBORAH T.	
	Examiner	Art Unit	
	Susan Y. Chen	2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

This office action is in response to amendment filed on 10/28/2005.

Claims 1, 3-11 and 13-21 are pending for examination. Claims 1, 10, 11 and 20 have been amended.

Terminal Disclaimer

The terminal disclaimer filed on 10/28/2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,658,447 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-11 and 13-21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (U.S. Patent. No. 6,105,127), in view of Olarig et al. (U.S. Patent No. 5,944,809).

Kimura et al's patent (EP 0827071 now U.S. Patent No. 6,105,127) was provided twice by applicant via IDS filed on 10/03/2001 and 08/07/2002.

As to claim 20, Kimura et al. (Thereinafter referred as Kimura) disclosed an apparatus for establish thread priority in a processor [Title; Abstract; Fig. 2] comprising:

a) a memory including Task priority Register (TPR) to store a value to indicate which one of the threads has a higher priority [e.g., Fig (s). 6-7; Fig. 15; col. 8, lines 59 – col. 9, line 8, etc.];

b) a resource allocated between the plurality of threads depending on a priority assigned to each thread in the memory [e.g., Abstract, lines 10-15; the shared resource functional unit, col. 6, lines 19-30; col. 8, lines 17-27].

Kimura does not expressly disclose a counter loaded with a predetermined value by control logic for each thread in the memory, such that the value being selected depending on the priority assigned, and the counter being used to allocate said resource between a plurality of threads.

However, Olarig et al. (hereinafter referred as Olarig) discloses a counter loaded with a predetermined value by control logic for each thread in the memory, such that the value being selected depending on the priority assigned [e.g., col. 3, lines 22-38; two-bit counter, at col. 6, lines 42-57], and the counter being used to allocate said resource between a plurality of threads [e.g., the LOPIC and COPIC processing via round robin arbitration protocol in Abstract; Fig(s) 1-3 and associated texts; Note: the round robin arbitration protocol is default implemented by a plurality of thread].

between a plurality of threads [e.g., the LOPIC and COPIC processing via round robin arbitration protocol in Abstract; Fig(s) 1-3 and associated texts; Note: the round robin arbitration protocol is default implemented by a plurality of thread].

Kimura and Olarig are in the same field of endeavor to optimize the performance of the extended multiprocessor system via controlling the interrupt signal flow among a plurality of thread processing. Thus, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kimura using the well-known counter as taught by Olarig to control the loading of a predetermined value by control logic for each thread in the memory, because by doing so, as suggested by Olarig the combined system would be able to use the counter to determine the overall priority level for a processing unit in a multiprocessing system and distribute the interrupt to that processing unit, therefore to balance the workload of the combined system [e.g., Olarig: col. 3, lines 18-38].

As to claim 11, this claim merely recited the same features as claim 20 with less limitations, hence are rejected for the same reason.

As to claims 13-19 and 21, in addition to the features of claims 11 and 20, Kimura and Olarig further disclosed that access to the resource is given to the thread with higher priority and the usage of the resource [e.g., Kimura: col. 4, line 64-col. 5, line 10; col. 6, lines 26-30], wherein the resource is a decode unit [Kimura: 1-3, Fig. 2; instruction decode units 1-3; Fig. 13; 111-113, Fig. 15] in a processor system, the

decode unit correspond to a bus unit [for example, Kimura: Internal Bus and Instruction Decode Units 1-3, Fig. 13] which including queues [for example, Kimura: 30, 40, 50, Fig. 2; 140, Fig. 15] to storing bus requests from a plurality of threads [Kimura: Fig. 2; Fig. 8; Fig. 11; Fig. 13] and control logic [Kimura: 60, Fig. 2; 60, 150, 170, Fig. 15] couple to the queues to select based on the priority value [Kimura: Fig. 2; Fig (s). 8-9; Fig. 11; Fig. 13; Fig. 15 and associated texts].

As to claims 1, 3-10, the steps in the claimed method is deemed to be made obvious by the functions of the apparatus structure of claims 11 and 13-20 in the combination discussed above, hence were rejected for the same reasons.

Response to Arguments

Applicant's arguments with respect to claims 1, 3-11 and 13-21 are based on amended subject matter that have been considered but are moot in view of the new ground(s) of rejection (i.e., 35 U.S.C. 112 second paragraph rejection).

Conclusion

To expedite the process of re-examination, the examiner requests that all future correspondences in regard to overcoming prior art rejections or other issues (e.g. 35 U.S.C. 112) set forth by the Examiner prior to the office action, that applicant should provide and link to the most specific page and line numbers of the disclosure where best support is found (see 35 U.S.C. 132).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Mayer et al. (U.S. Patent No. 6,249,830) which discloses a system to process computer instructions via multi-thread and program counter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Susan Y. Chen whose telephone number is 571-272-4016. The examiner can normally be reached on Monday - Friday from 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 571-272-4023. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Susan Y Chen
Examiner
Art Unit 2161

December 28, 2005

UYEN LE
PRIMARY EXAMINER